UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,203	02/10/2005	Hiroaki Ozeki	MAT-8657US	9927

23122 7590 07/13/2010

RATNERPRESTIA
P.O. BOX 980
VALLEY FORGE, PA 19482

EXAMINER	
TIMORY, KABIR A	
ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
07/13/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/524,203	OZEKI ET AL.	
	Examiner	Art Unit	
	KABIR A. TIMORY	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. This office action is in response to the amendment filed on 04/27/2010. Claims 1-11 are pending in this application and have been considered below.

2. Applicant's arguments with respect to claim 1 and have been considered but are moot in view of new ground(s) of rejection because of the amendments.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (US 6075829) in view of Paneth et al. (US 4862107) and further in view of Applicant's Admitted Prior Art (AAPA) (figure 5, specification, page 1, lines 10-27, and page 2, lines 1-2) and Messer et al. (US 5113189).

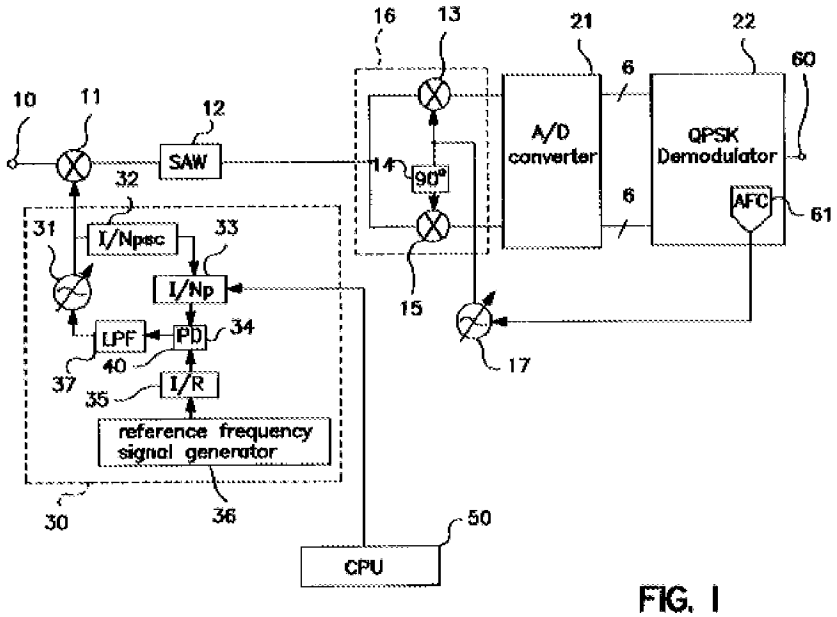


FIG. 1

Regarding claim 1:

As shown in figures 1-16, Hayashi et al. disclose a digital signal receiver **(abstract)** comprising:

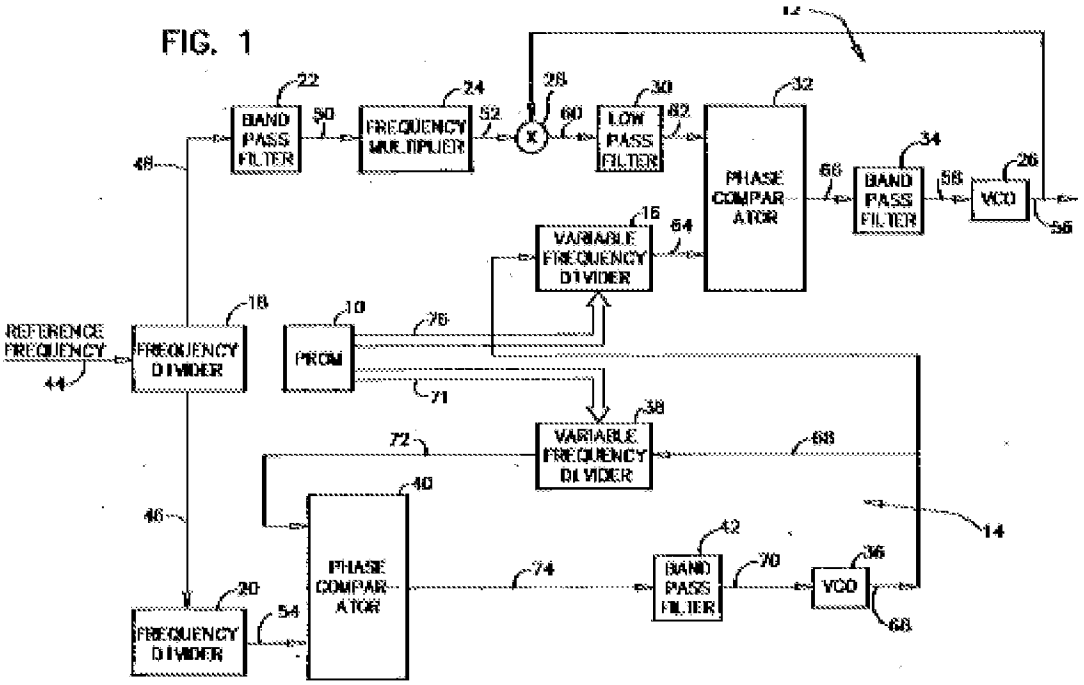
- a reference signal generator **(36 in figure 1)** for generating a first reference signal **(col 5, lines 5-7)**;
- a base band transform circuit **(16 in figure 1)** for converting a first high-frequency signal with digital modulation into a base band signal with using the first reference signal (**On page 3 of the specification of the instant application, lines 9-14, the applicant discloses:** "Base-band orthogonal transform circuit 3 converts a frequency of the intermediate frequency signal output from frequency converter 2 into base-band orthogonal signals including base-band I signal 14 and base-band Q signal 15 with using the reference signal generated by reference signal generator 1". **In figure 1, Hayashi et al. clearly shows that orthogonal detector 16 is receiving the IF signal output from the frequency converter 11 via filter 12 and convert the received IF signal into in-phase (I) and quadrature (Q)**

base-band signal (see col 4, lines 35-43). Therefore, the examiner makes his broadest reasonable interpretation in light of the specification that the orthogonal detector 16 of Hayashi et al. to be the base band transform circuit); and

- wherein the first reference signal is generated independent of the signal output of the frequency multiplier **(figure 1 shows that the reference signal is generated independently)**.

Hayashi et al. discloses all of the subject matter as described above except for specifically teaching a frequency divider to divide a frequency of the first reference signal; a frequency multiplier wherein an output frequency of the frequency multiplier is a product of a multiplicand value which is the divided frequency of the first reference signal produced by the frequency divider and a multiplier value of the frequency multiplier, and wherein the first reference signal divided by the frequency divider is input only to the frequency multiplier.

However, Paneth et al. in the same field of endeavor teaches a frequency divider **(18 in figure 1)** to divide a frequency of the first reference signal **(44 in figure 1)**; a frequency multiplier **(24 in figure 1)** wherein an output frequency of the frequency multiplier **(52 in figure 1)** is a product of a multiplicand value **(multiplying the frequency of the signal by nine is interpreted to be the multiplicand value)** which is the divided frequency of the first reference signal **(44 in figure 1)** produced by the frequency divider **(18 in figure 1)** and a multiplier value **(multiplying the frequency of the signal by nine is interpreted to be the multiplicand value)** of the frequency multiplier **(24 in figure 1) (col 3, lines 10-29)**.

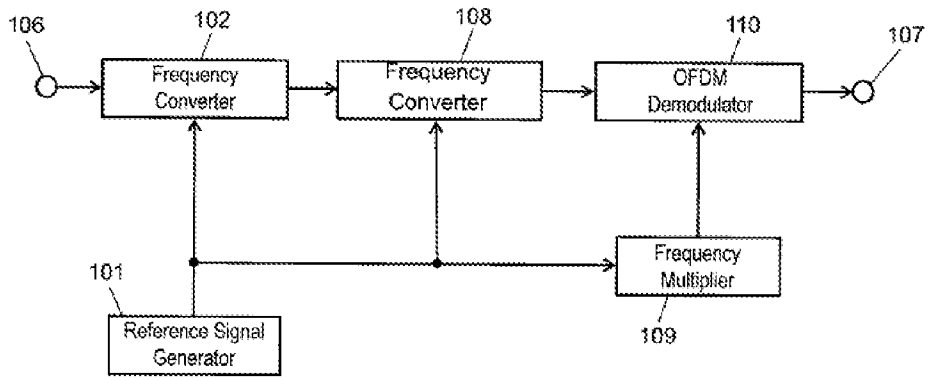


Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a frequency divider at the input of a frequency multiplier as taught by Paneth et al. to combine and modify the system and method of (AAPA) in order to divided signal at a predetermined frequency and to provide a frequency reference signal at a predetermined frequency.

Although Hayashi et al. discloses a digital demodulator **(22 in figure 1)** to demodulate a signal output from the base band transform circuit **(16 in figure 1)**, he fails to teach to demodulate with using the signal output from the frequency multiplier as a reference signal, and wherein the first reference signal divided by the frequency divider is input only to the frequency multiplier.

However, AAPA et al. in the same field of endeavor teaches to demodulate **(110 in figure 5)** with using the signal output from the frequency multiplier **(109 in figure 5)** as a reference signal **(see figure 5)**.

FIG. 5 PRIOR ART



Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a frequency multiplier as taught by AAPA to combine and modify the system and method of Hayashi et al. in order to convert the frequency of the reference signal.

Hayashi et al., Paneth et al., and AAPA disclose all of the subject matter as described above except for specifically teaching wherein the first reference signal divided by the frequency divider is input only to the frequency multiplier.

However, Messer et al. in the same field of endeavor teaches wherein the first reference signal **(F_{CLK} in figure 1)** divided by the frequency divider **(14 in figure 1)** is input only to the frequency multiplier **(16 in figure 1) (col 3, lines 16-65)** ***(KSR – combining prior art elements according to known method to yield predictable results)***.

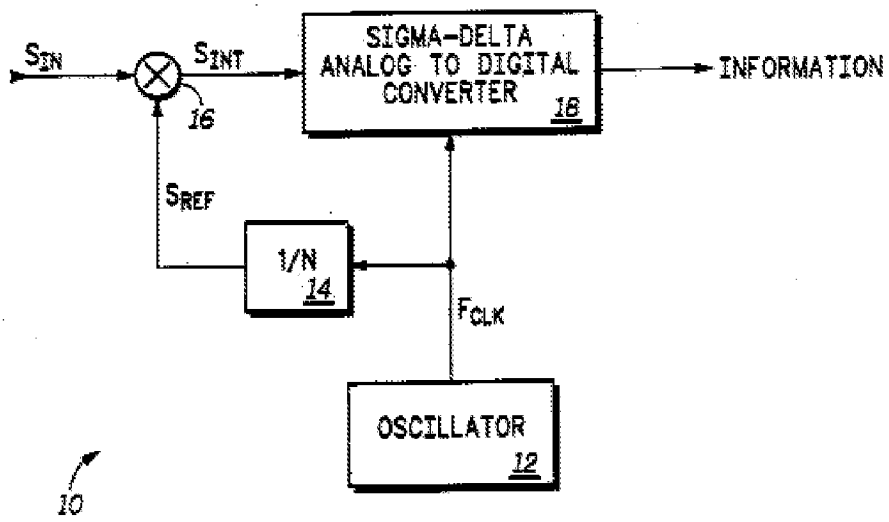


FIG.1

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use the frequency divider as taught by Messer to combine and modify the system and method of Hayashi et al. in order to divide the frequency by an integer value of N which will ensure that the output of the frequency multiplier is within a predetermined range of frequency **(col 4, lines 34-40)**.

Regarding claim 2:

Hayashi et al. further discloses a frequency converter **(11 in figure 1)** for receiving a second high-frequency signal modulated by the digital signal and converting a frequency of the second high-frequency signal to generate the first high-frequency signal **(col 4, lines 33-52)**.

Regarding claim 3:

Hayashi et al. further discloses wherein the frequency converter converts the second high-frequency signal into the first high-frequency signal with using the first reference signal **(figure 1 shows that frequency converter 11 uses the reference signal provide by the reference signal generator 36. See figure 1 above) (col 4, lines 33-52)**.

Regarding claim 4:

Hayashi et al. and Paneth et al. disclose all of the subject matter as described above except for specifically teaching wherein the first high-frequency signal is modulated by the digital signal by Orthogonal Frequency Division Multiplexing system, and the digital demodulator comprises an Orthogonal Frequency Division Multiplexing demodulator.

However, AAPA et al. in the same field of endeavor teaches wherein the first high-frequency signal is modulated by the digital signal by Orthogonal Frequency Division Multiplexing system **(110 in figure 5)**, and the digital demodulator comprises an Orthogonal Frequency Division Multiplexing demodulator **(specification, page 1, lines 10-27, and page 2, lines 1-2)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a Orthogonal Frequency Division Multiplexing demodulator as taught by AAPA to combine and modify the system and method of Hayashi et al. in order to demodulate high-frequency signal digitally.

Regarding claim 5:

Hayashi et al. further discloses wherein the base band transform circuit **(16 in figure 1)** comprises an orthogonal base band transform circuit **(13-15 in figure 1)** operable to convert the first high-frequency signal into a first base band signal **(in-phase I component)** and a second base band signal **(Quadrature Q component)** orthogonal each other and output the first base band signal and the second base band signal **(col 4, lines 35-52)**.

Regarding claim 6:

Hayashi et al. further discloses wherein the orthogonal base band transform circuit includes a 90°-phase shifter for shifting a phase of the first reference signal by 90 degrees **(14 in figure 1 provides 90° phase shift for the system)**, a first mixer **(13 in figure 1)** for mixing the first reference signal with the first high-frequency signal to convert the first high-frequency signal into the first base band signal, and a second mixer **(15 in figure 1)** for mixing the second reference signal with the first high-frequency signal to convert the first high-frequency signal into the second base band signal **(col 4, lines 35-52, col 5, lines 22-36)**.

Regarding claim 9:

Hayashi et al. disclose all of the subject matter as described above except for specifically teaching a low-pass filter for receiving a signal output from the frequency divider and outputting a signal to the frequency multiplier.

However, Paneth et al. in the same field of endeavor teaches a low-pass filter **(22 in figure 1)** for receiving a signal output from the frequency divider **(18 in figure 1)** and outputting a signal to the frequency multiplier **(24 in figure 1)**. ***Although, block 22 of figure 1 shows band pass filter, however, it would have been obvious to one of ordinary skilled in art to substitute the band pass filter with a low-pass filter to obtain a predictable result) (KSR – simple substitution of one known element for another to obtain predictable results)***. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use the filter as taught by Paneth et al. to combine and modify the system and method of (AAPA) in order to minimize phase noise and electronic noise of the system (see col 1, lines 50-53).

Regarding claim 10:

(AAPA) further discloses a further device including the digital demodulator **(110 in figure 5)** and the frequency multiplier **(109 in figure 5)**.

5. Claims 7-8 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. in view of Paneth et al. and Applicant's Admitted Prior Art (AAPA) and Messer et al. as applied to claim 1 above and further in view of Lee et al. (US 20010048715).

Regarding claims 7 and 11:

Hayashi et al., Paneth et al., and AAPA et al. discloses all of the subject matter as described above except for specifically teaching wherein the frequency divider and at least one of the base band transform circuit and the frequency converter are formed in a bi-COMOS device.

However, Lee et al. in the same field of endeavor teaches wherein the frequency divider and at least one of the base band transform circuit and the frequency converter are formed in a bi-COMOS device **(par 0007)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use bi-CMOS device as taught by Lee et al. to combine and modify the system and method of (AAPA) in order to provide better speed and noise characteristics.

Regarding claims 8 and 10:

AAPA et al. further discloses wherein the digital demodulator **(110 in figure 5)** and the frequency multiplier are formed in a CMOS device **(par 0008-0009)**. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use CMOS device as taught by Lee et al. to combine and modify the system and method of (AAPA) in order to reduce the cost, size and power consumption (par 0005)

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KABIR A. TIMORY whose telephone number is (571)270-1674. The examiner can normally be reached on 8:00 AM - 4:30 PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kabir A Timory/
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611